Freescale Semiconductor
Product Brief

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MPC8569E PowerQUICC™ III Integrated Processor Product Brief

This document provides an overview of the features and functionality of the MPC8569E PowerQUICC™ III integrated communications processor. This device combines an e500 processor core built on Power Architecture™ technology with system logic required for networking, wireless infrastructure, and telecommunications applications.

The MPC8569E offers an excellent combination of protocol and interface support, including a high-performance CPU with large L2 cache, one 64-bit or two 32-bit DDR2/DDR3 memory controllers, SGMII, serial RapidIO™, USB 2.0, and PCI Express®. These features allow the replacement of separate control and data path processors with a single chip. The MPC8569E also incorporates the new QUICC Engine™ block with four RISC processors, which provide termination, interworking, and switching between a wide range of communication protocols, including ATM, Ethernet, POS, and HDLC. The QUICC Engine block's enhanced interworking eases the transition from ATM to IP-based

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systems and reduces investment costs. The MPC8569E also supports the IEEE 1588™ precision time protocol for network synchronization over Ethernet.

1 MPC8569E Overview

This section describes the features of the MPC8569E.

1.1 Block Diagram

Figure 1 shows the major functional units within the MPC8569E.

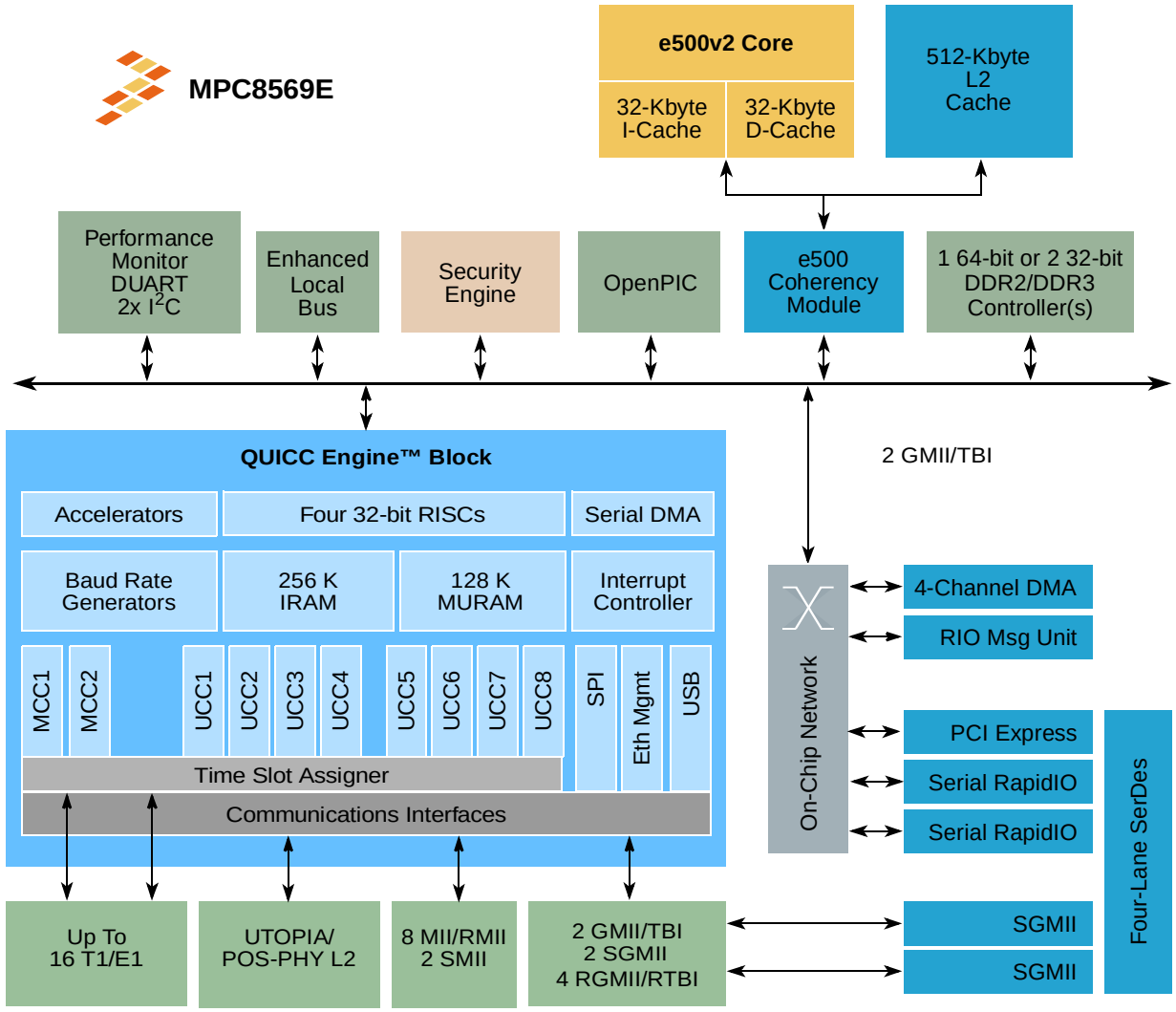

Figure 1. MPC8569E Block Diagram

1.2 Critical Performance Parameters

The critical performance parameters for the MPC8569E are as follows:

- e500v2 core frequency of 1.33 GHz
- Power consumption of less than 7 W at 800 MHz core speed
- 45-nm SOI process technology
- Data rate of up to 800 Mbps/pin for DDR2 and DDR3
- Maximum QUICC Engine frequency of 667 MHz
- Supply voltages:
  - Core: 1.0 V
  - PCI Express, serial RapidIO: 1.0 V
  - Ethernet: 3.3 or 2.5 V (subject to protocol)
  - Local bus: 3.3, 2.5, or 1.8 V
  - DDR: 1.8 V for DDR2, 1.5 V for DDR3 (conforms to JEDEC standard)
- Operating junction temperature (T_j) range: 0–105°C
- Package: 783-pin, flip-chip PBGA

1.3 Chip-Level Features

Key features of the MPC8569E include:

- High-performance Power Architecture e500v2 core
  - 36-bit physical addressing
  - Double-precision floating-point support
- 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache
- 512-Kbyte L2 cache with ECC
- QUICC Engine block
  - Four RISC processors
  - Supports Ethernet, ATM, POS, and T1/E1 along with associated interworking
    - Four Gigabit Ethernet interfaces (up to two with SGMII)
    - Up to eight 10/100-Mbps Ethernet interfaces
    - Up to 16 T1/E1 TDM links (512 × 64 channels)
    - Multi-PHY UTOPIA/POS-PHY L2 interface (16-bit)
  - IEEE 1588 v2 support
  - SPI and Ethernet PHY management interface
  - Full-speed USB 2.0 interface
  - General-purpose I/O signals
- Integrated security engine
  - Protocol support includes ARC4, 3DES, AES, RSA/ECC, RNG, Single-pass SSL/TLS, Kasumi, SNOW, XOR acceleration

- One 64-bit or two 32-bit DDR2/DDR3 SDRAM memory controllers with ECC support
- High-speed interfaces:
  - Two ×1 serial RapidIO interfaces (with message unit) or one x4 interface
  - ×4/×2/×1 PCI Express interface
  - Two SGMII interfaces
  - Four-lane SerDes with the mux options shown in Table 1 (in Section 3.6.3, "High-Speed Interface Multiplexing")
- Programmable interrupt controller (PIC) compliant with Open-PIC standard
- Four-channel DMA controller
- Two I^2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)

These features are described in greater detail in subsequent sections.

NOTE

The MPC8569E is also available without a security engine, in a configuration known as the MPC8569. All specifications other than those relating to security apply to the MPC8569 exactly as described in this document.

2 MPC8569E Application Examples

The following section provides block diagrams of different MPC8569E applications. The MPC8569E is a very flexible device and can be configured to meet many system application needs.

2.1 Base Station Network Interface Card

Figure 2 shows an application using the MPC8569E as a base station network interface card.

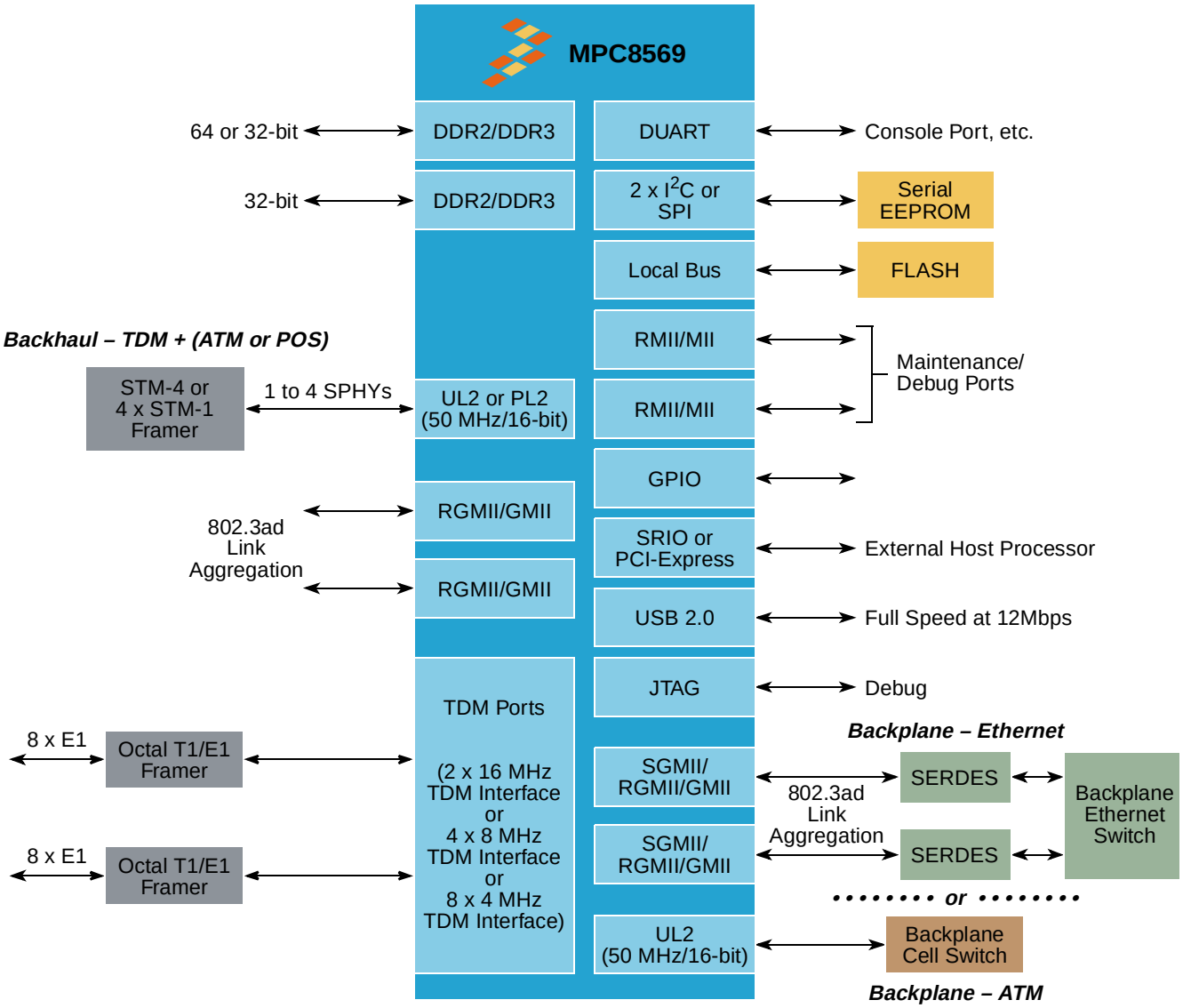

Figure 2. Base Station Network Interface Card Application

The MPC8569E enables glueless connection to an external host processor using PCI Express or a serial RapidIO interconnect in applications where a separate processor is used for control processing.

Support for both legacy ATM backplanes as well as gigabit Ethernet backplanes is provided. A UTOPIA Level 2 interface facilitates connection to an ATM backplane with a rich set of ATM TM4.1-compliant traffic management capabilities. When using an Ethernet backplane, the QUICC Engine technology offers an advanced Ethernet scheduler with the hard QoS capabilities necessary for mirroring the traffic management capabilities of ATM when migrating from ATM to Ethernet backplanes. Additionally, Ethernet multicast capabilities are also offered to offload multicasting from the CPU core to the QUICC Engine block for emerging video and streaming data services to mobile users. Furthermore, Ethernet link aggregation is offered to help attain a desired combination of higher throughput, load balancing, and redundancy.

For backhaul from a Node B to an RNC, connectivity of up to 16 T1/E1s through external framers is possible. Both IMA and MLPPP are supported on these links. The MPC8569E also supports a network interface card configuration for a Hub Node B. Such a hub aggregates T1/E1s from several subtended Node Bs and backhauls the traffic by ATM or POS over an STS-3c/STM-1 link. The QUICC Engine block supports the STS-3c/STM-1 by a UTOPIA/Packet-over-SONET (POS) Level 2 interface. Furthermore, backhaul by fast or gigabit Ethernet interfaces is also possible.

In addition to the variety of interface options, advanced multiprotocol interworking capabilities such as IMA to Ethernet interworking and MLPPP to Ethernet interworking are also offerred. Designed with IPv6 support in mind, powerful protocol handling capabilities at Layers 2, 3, and 4 facilitate the migration towards an All-IP network A flexible and programmable solution for the network interface card is highly desirable to facilitate feature additions as standards and system architectures evolve. Hence the MPC8569E offers a complete solution to meet different network interface card architectures.

2.2 UMTS Channel Card

Figure 3 shows the MPC8569E used as a UMTS channel card.

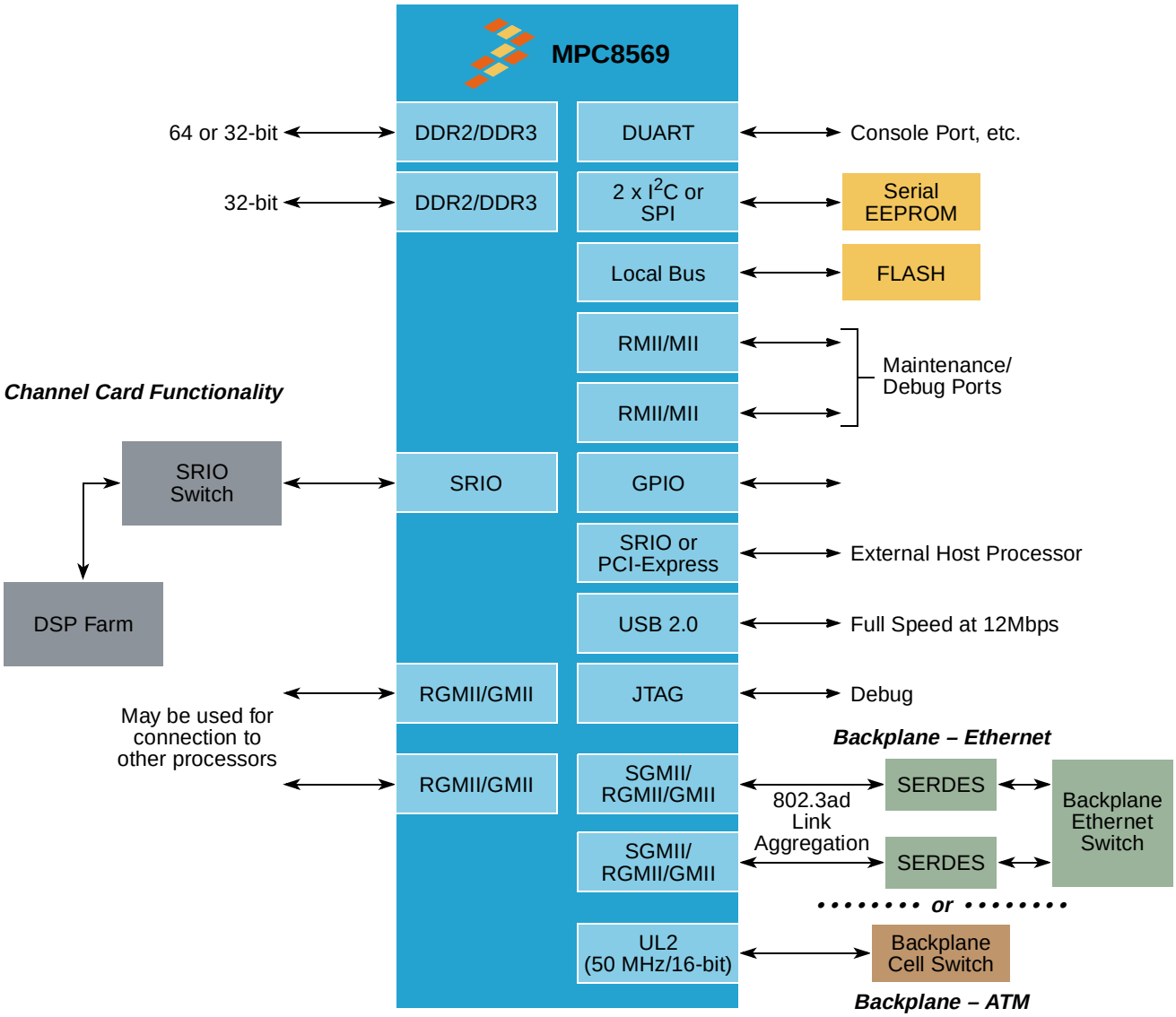

Figure 3. UMTS Channel Card Application

In a channel card, the MPC8569E performs the data path functionality between the baseband processing DSPs on the channel card and network interface cards. Options for connectivity over the backplane are as described in Section 2.1, “Base Station Network Interface Card,” and include both ATM and Ethernet backplanes. Connections to DSPs are typically achieved by Ethernet or serial RapidIO interfaces. A ×1 or ×4 serial RapidIO interface may be used to connect to a RapidIO switch. The switch, in turn, connects to multiple DSPs. Alternatively, two ×1 serial RapidIO interfaces, which are offered on the MPC8569E, may be used to connect to two multicore baseband processing DSPs directly. The two ×1 serial RapidIO interfaces also can facilitate an efficient daisy chain across a chain of DSPs without a switch.

3 MPC8569E Architecture Overview

This section contains a high-level view of the MPC8569E architecture.

3.1 e500v2 Core and Memory Unit

The MPC8569E contains a high-performance, 32-bit, Power instruction set architecture (ISA)–enhanced e500v2 core that implements Power Architecture technology. In addition to 36-bit physical addressing, this version of the e500 core includes:

- Embedded floating-point instructions defined as part of the SPE that use the general-purpose registers (GPRs) for specifying operands. These include the following:
  - 64-bit vector and 32-bit scalar single-precision floating-point instructions
  - 64-bit, scalar, double-precision floating-point instructions
- 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection

The MPC8569E also contains 512 Kbytes of L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- SRAM features include the following:
  - I/O devices access SRAM regions by marking transactions as snoopable (global).
  - Regions can reside at any aligned location in the memory map.
  - Byte-accessible ECC uses read-modify-write transaction accesses for smaller-than-cache-line accesses.

3.2 e500 Coherency Module (ECM) and Address Map

The e500 coherency module (ECM) provides a mechanism for I/O-initiated transactions to snoop the bus between the e500v2 core and the integrated L2 cache in order to maintain coherency across local cacheable memory. It also provides a flexible switch-type structure for core- and I/O-initiated transactions to be routed or dispatched to target modules on the device.

The MPC8569E supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space. The local address map is supported by ten local access windows that define mapping within the local 36-bit (64-Gbyte) address space.

The MPC8569E can be made part of a larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allows the MPC8569E to be part of larger address maps such as those of PCI Express or RapidIO.

3.3 QUICC Engine Block

The QUICC Engine block includes support for the following:

- Serial interfaces
  - UTOPIA/POS-PHY L2 bus controller (UPC) supporting 124 ports (optional 128 ports with extended address)
  - Up to four gigabit Ethernet interfaces. The following combinations are supported:
    - Four RGMII/RTBI
    - Two RGMII/RTBI and two SGMII
    - Two RGMII/RTBI and one GMII
    - Two GMII and two SGMII
  - Up to eight 10/100-Mbps Ethernet interfaces using RMII
  - Up to 16 T1/E1/J1/E3 or DS-3 serial interfaces
  - SPI and Ethernet PHY management interface
  - One full-/low-speed USB interface supporting USB 2.0
- Protocols
  - IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
  - L2 Ethernet switching using MAC address or IEEE 802.1P/Q® VLAN tags
  - IP forwarding
  - ATM SAR up to 622 Mbps (OC-12) full duplex, with ATM traffic shaping (ATM Forum TM 4.1) for up to 64K ATM connections
  - ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
  - IMA and ATM transmission convergence sub-layer
  - ATM OAM handling features compatible with ITU-T I.610
  - PPP, multi-link (ML-PPP), multi-class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
  - ATM (AAL2/AAL5) to Ethernet (IP) interworking
  - PPP to Ethernet interworking
  - Extensive support for ATM statistics and Ethernet RMON/MIB statistics
  - 512 channels of HDLC/Transparent or 256 channels of SS7
- IEEE 1588 v2 support

3.4 Integrated Security Engine (SEC)

The SEC is a modular and scalable security core optimized to process all the algorithms associated with IPsec, IKE, SSL/TLS, iSCSI, SRTP, IEEE 802.11i®, IEEE 802.16® (WiMAX), IEEE 802.1AE® Std. (MACSec), 3GPP, A5/3 for GSM and EDGE, and GEA3 for GPRS. Although it is not a protocol processor, the SEC is designed to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a

single pass of the data. The version of the SEC used in the MPC8569E is specifically capable of performing single-pass security cryptographic processing for SSL 3.0, SSL 3.1/TLS 1.0, IPSec, SRTP, and 802.11i.

SEC features include the following:

- Compatible with code written for the Freescale MPC8548E, MPC8555E, and MPC8541E devices
- XOR engine for parity checking in RAID storage applications.
- Four crypto-channels, each supporting multi-command descriptor chains
- Cryptographic execution units:
  - PKEU—public key execution unit
  - DEU—data encryption standard execution unit
  - AESU—advanced encryption standard unit
  - AFEU—ARC four execution unit
  - MDEU—message digest execution unit
  - KEU—Kasumi execution unit
  - CRCU—cyclical redundancy check unit
  - RNG—random number generator
  - SEU—SNOW standard execution unit

3.5 DDR SDRAM Controllers

The MPC8569E has one 64-bit or two 32-bit DDR controllers, which support DDR2 and DDR3 SDRAM. The memory interfaces control main memory accesses and provide for a maximum of 16 Gbytes of main memory.

The MPC8569E supports a variety of SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities from 64 Mbits to 4 Gbits. Four chip select signals support up to four banks of memory. The MPC8569E supports bank sizes from 64 Mbytes to 4 Gbytes. Nine column address strobes ($\overline{\text{MDM}}$[0:8]) are used to provide byte selection for memory bank writes.

The MPC8569E can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 16 simultaneously open pages (32 for DDR2/DDR3) can dramatically reduce access latencies for page hits. Depending on the memory system design and timing parameters, using page mode can save 3 to 4 clock cycles from subsequent burst accesses that hit in an active page.

Using ECC, the MPC8569E detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

The MPC8569E can invoke a level of system power management by asserting the MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode.

The MPC8569E offers both hardware and software options to support battery-backed main memory. In addition, the DDR controller offers an initialization bypass feature that system designers may use to prevent re-initialization of main memory during system power-on following abnormal shutdown.

3.6 High Speed I/O Interfaces

The MPC8569E supports the SGMII, serial RapidIO, and PCI Express high-speed I/O interface standards.

3.6.1 Serial RapidIO

The serial RapidIO interface is based on the *RapidIO Interconnect Specification, Revision 1.2*. RapidIO is a high-performance, point-to-point, low-pin-count, packet-switched system-level interconnect that can be used in a variety of applications as an open standard. The RapidIO architecture has a rich variety of features including high data bandwidth, low-latency capability, and support for high-performance I/O devices, as well as support for message-passing and software-managed programming models. Key features of the serial RapidIO interface unit include:

- Support for *RapidIO Interconnect Specification, Revision 1.2* (all transaction flows and priorities)
- Both ×1 and ×4 LP-serial link interfaces, with transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
- Auto detection of ×1 or ×4 mode operation during port initialization
- 34-bit addressing and up to 256-byte data payload
- Receiver-controlled flow control
- Support for RapidIO error injection
- Internal LP-serial and application interface-level loopback modes

The RapidIO messaging unit supports two inbox/outbox mailboxes (queues) for data and one doorbell message structure. Both chaining and direct modes are provided for the outbox, and messages can hold up to 16 packets of 256 bytes, or a total of 4 Kbytes.

3.6.2 PCI Express Interface

The MPC8569E supports a PCI Express interface compliant with the *PCI Express Base Specification Revision 1.0a*. It is configurable at boot time to act as either root complex or endpoint.

The physical layer of the PCI Express interface operates at a 2.5-Gbaud data rate per lane. The theoretical unidirectional peak bandwidth is 2 Gbps per lane. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 4 Gbps per lane.

Other features of the PCI Express interface include:

- ×4, ×2, and ×1 link widths supported
- Both 32- and 64-bit addressing and 256-byte maximum payload size
- Full 64-bit decode with 36-bit wide windows

3.6.3 High-Speed Interface Multiplexing

Table 1 shows the supported high-speed interface configurations. The desired configuration must be selected at power-on reset.

Table 1. Supported High-Speed Interface Combinations

Configuration	Lanes				Frequency
	f	e	b	a	
1	SGMII	SGMII	×1 SRIO2	×1 SRIO1	SRIO at 2.5 Gbaud
2	SGMII	SGMII	—	×1 PEX	PEX at 2.5 Gbaud
3	SGMII	SGMII	×2 PEX		PEX at 2.5 Gbaud
4	×1 SRIO2	×1 SRIO1	—	×1 PEX	2.5 Gbaud
5	×1 SRIO2	×1 SRIO1	×2 PEX		2.5 Gbaud
6	×4 SRIO1				2.5 or 3.125 Gbaud
7	×4 PEX				2.5 Gbaud
8	—	—	—	×1 PEX	2.5 Gbaud
9	—	—	×1 SRIO2	×1 SRIO1	3.125 Gbaud
10	SGMII	SGMII	×1 SRIO2	×1 PEX	SRIO at 2.5 Gbaud

3.7 Programmable Interrupt Controller (PIC)

The MPC8569E PIC implements the logic and programming structures of the OpenPIC architecture, providing for external interrupts (with fully nested interrupt delivery), message interrupts, internal-logic driven interrupts, and global high-resolution timers. Up to 16 programmable interrupt priority levels are supported. The PIC can be bypassed to allow use of an external interrupt controller.

3.8 DMA, I^2C, DUART, and Enhanced Local Bus Controller

The MPC8569E provides an integrated four-channel DMA controller, which can transfer data between any of its I/O or memory ports or between two devices or locations on the same port. The DMA controller can be used as follows:

- To chain (both extended and direct) through local memory-mapped chain descriptors.
- To handle misaligned transfers as well as stride transfers and complex transaction chaining.
- To specify local attributes such as snoop and L2 write stashing.

There are two I^2C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. Both the transmitter and receiver support 16-byte FIFOs.

The MPC8569E enhanced local bus controller (eLBC) port allows connection with a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine

(GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user programmable machine (UPM) can be programmed to interface to synchronous devices or custom ASIC interfaces. The NAND Flash control machine (FCM) further extends interface options. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM, UPM, or FCM controller. All may exist in the same system. The local bus controller supports the following features:

- Nonmultiplexed bus: 28-bit address and 16-bit data, operating at up to 166 MHz
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- 16- and 8-bit port sizes controlled by on-chip memory controller
- Three protocol engines available on a per-chip-select basis
- Parity support
- Default boot ROM chip select with configurable bus width (8 or 16 bits)
- Supports zero-bus-turnaround (ZBT) RAM
- Boot from 8-bit NAND Flash

3.9 Device Boot Locations

The MPC8569E may be configured to boot using one of the following interfaces:

- DDR2/DDR3 memory controller
- Serial RapidIO interface
- PCI Express interface
- Local bus interface (using the GPCM)
- I^2C boot sequencer (I^2C1 interface)
- SD/MMC controller

3.10 Power Management

In addition to low-voltage operation and dynamic power management, which automatically minimizes power consumption of blocks when they are idle, four power consumption modes are supported: full on, doze, nap, and sleep.

3.11 System Performance Monitor

The performance monitor facility supports eight 32-bit counters that can count up to 512 counter-specific events. It supports duration and quantity threshold counting and a burstiness feature that permits counting of burst events with a programmable time between bursts.

4 Development Environment

Development tools, hardware platforms, software building blocks, and application-specific software solutions are available from Freescale and the Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

4.1 Software Development Tools

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator, and debugger for the e500v2 core.

4.2 Modular Development System (MDS)

Freescale provides an MDS board as a reference platform and programming development environment for the MPC8569E with a complete Linux board support package. The MDS board supports on-board DDR SDRAM memory and a debug port and can be configured with optional daughter cards supporting protocols such as OC-3 or OC-12 ATM, 16x T1/E1, and Ethernet (10/100/1000Base T).

4.3 Modular Software Building Blocks

The QUICC Engine block is supported by a complete set of configurable device API drivers and initialization software. Table 2 and Table 3 show the wealth of software protocols that the QUICC Engine block with the e500v2 core supports.

Table 2. QUICC Engine Block Software Package Overview: Demo Applications and Drivers

Category	Example	Documentation
Demo Applications	(Node B, DSLAM, DSP Aggregator, WAN GW)	Demo Manuals, Use cases HOW TOs
Driver applications	Use cases, Test application suite	Tests reports
Termination Drivers	ATM, ETH, Interworking Drivers	Drivers API

Table 3. QUICC Engine Block Software Package Overview: MIcrocode

Layer	Use
Layer 3+	**Layer 3 (IP/Ethernet)** L3 control packets filtered to host CPU Parsing & Multi-field classification Hierarchical Lookups **Traffic Management (IP/Ethernet)** Combined SP + WFQ Scheduling Rate limiting/shaping Lossless Flow Control DiffServ + WRED **ATM** TM 4.1 UBR, CBR, GFR, VBR Per-flow ATM scheduler for 64K VC's Hierarchical frame and cell based scheduling Policing Congestion Control
Layer 2.5	VLAN ATM to ATM switching ATM to Ethernet interworking AAL2 CPS switching and SSSAR Multi-Link PPP, Multi-Class PPP, PPP-Mux PPP to Ethernet interworking IP Header Compression IMA over TDM / UTOPIA / Channelized E-MSP
Layer 2	ATM AAL 0/1/2/5 10/100/1000 Ethernet L2 (Fast Ethernet) Switch HDLC BISYNC Serial ATM (ATM TC sublayer) SS7
Layer 1 (Physical)	UTOPIA-L2, POS-L2 10/100/1000 Ethernet TDM – T1/T3/E1/E3

5 Document Revision History

Table 4 provides a revision history for this product brief.

Table 4. Document Revision History

Rev. No.	Date	Substantive Change(s)
0	2/2009	This is the first released version of this document.

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USA/Europe or Locations Not Listed:
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Technical Information Center, EL516
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Europe, Middle East, and Africa:
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Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
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Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

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